a first dummy gate arranged between said first drain and said second source;

a second dummy gate arranged adjacent to said first source; and

a third dummy gate arranged adjacent to said second drain,

wherein said first and second gates, and said first, second and third dummy gates are substantially evenly spaced.

4. (Amended) The semiconductor device according to claim 3, wherein a first distance between said first gate and said first dummy gate and a second distance between said second gate and said first dummy gate are substantially the same as each other, and

wherein said first and second gates are respectively three-forked.

5. (Amended) A semiconductor device comprising:

a first transistor having

a first source,

a first drain,

a first gate arranged between said first source and said first drain,

a first contact hole formed on said first source and arranged at a first distance from said first gate, and

a second contact hole formed on said first drain and arranged at a second distance from said first gate, said second distance being the same as said first distance;

a second transistor having

a second source,

a second drain,

a second gate arranged between said second source and second drain,

a third contact hole formed on said second source and arranged at a third distance from said second gate, and

a fourth contact hole formed on said second drain and arranged at a fourth distance from said second gate, said fourth distance being the same as said third distance;

a first dummy gate set between said first drain and said second source;

a second dummy gate set next to said first source; and

a third dummy gate set next to said second drain,

wherein said first gate, said second gate, said third gate, said first dummy gate, said second dummy gate, and said third dummy gate are substantially evenly spaced.

6. (Amended) A semiconductor device including first and second transistors each having a terminal commonly connected to a node, said device comprising:

a first gate electrode layer of said first transistor;

a first electrode layer of said first transistor coupled to a first contact hole;

a second electrode layer of said first transistor coupled to a second contact hole;

a second gate electrode layer of said second transistor, said second gate electrode layer being electrically separated from said first gate electrode layer;

a third electrode layer of said second transistor coupled to a third contact hole;

a fourth electrode layer of said second transistor coupled to a fourth contact hole, said fourth electrode layer electrically coupled to said second electrode layer as said terminal,

wherein said first gate electrode layer, said first electrode layer, said second electrode layer, said second gate electrode layer, said third electrode layer, and said fourth electrode layer are arranged so that a first distance between said first contact hole and said first gate electrode layer is substantially the same as a second distance between said third contact hole and said second gate electrode, and a third distance between said second contact hole and said first gate electrode layer is substantially the same as a fourth distance between said fourth contact hole and said second gate electrode layer while a mask for forming said first to fourth contact holes is misaligned

11. (Amended) A semiconductor device, comprising:

a first source diffusion region;

a first drain diffusion region;

a second source diffusion region;

a second drain diffusion region,

said first source diffusion region, said first drain diffusion region, said second source diffusion region, and said second drain diffusion region being arranged in that order on

a line extending in a first direction, said first and second source diffusion regions and said first and second drain diffusion regions being surrounded by an element isolation region;

a first gate electrode formed between said first source and drain diffusion regions and extending in a second direction extending in said second direction;

a first second gate electrode formed between said second source and drain diffusion regions and extending in said second direction;

a first source electrode formed over said first source diffusion region and connected with said first source diffusion region through a first contact hole;

a first drain electrode formed over said first drain diffusion region and connected with said first drain diffusion region through a second contact hole;

a second source electrode formed over said second source diffusion region and connected with said second source diffusion region through a third contact hole;

a second drain electrode formed over said second drain diffusion region and connected with said second drain diffusion region through a fourth contact hole;

cont.

a first dummy gate electrode arranged between said first drain and said second source electrodes on said element isolation region;

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a second dummy gate electrode arranged on said element isolation region so that said first source electrode is sandwiched between said second dummy gate electrode and said first gate electrode; and

a third dummy gate electrode arranged on said element isolation region so that said second drain electrode is sandwiched between said third dummy gate electrode and said second gate electrode,

wherein a first distance between said first dummy gate electrode and said first gate electrode and a second distance between said first dummy gate electrode and said second gate electrode are substantially the same as each other.

Please add new claims 13 - 25 as follows:

- - 13. (New) The semiconductor device according to claim 4, wherein a third distance between said second dummy gate and said first gate and a fourth distance between said third dummy gate and said second gate are substantially the same as each other.

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14. (New) The semiconductor device as claimed in claim 5, wherein said first source, said first drain, said second source, and said second drain are arranged in this order.

15. (New) The semiconductor device as claimed in claim 14, wherein said first gate and said second gate have a same length and width as each other.

16. (New) The semiconductor device as claimed in claim 11, further comprising:

a first lead-out contact hole connected to said first gate electrode, and arranged on said element isolation region;

a second lead-out contact hole connected to said second gate electrode, and arranged on said element isolation region; and

a first dummy lead-out contact hole connected to said first dummy gate electrode, and arranged on said element isolation region,

wherein said first lead-out contact hole, said second lead-out contact hole, and said first dummy lead-out contact hole are arranged in one line of said first direction.

17. (New) The semiconductor device as claimed in claim 16, further comprising:

a second dummy lead-out contact hole connected to said second dummy gate electrode, and arranged on said element isolation region; and

a third dummy lead-out contact hole connected to said third dummy gate electrode, and arranged on said element isolation region,

wherein said first lead-out contact hole, said second lead-out contact hole, said first dummy lead-out contact hole, said second dummy lead-out contact hole, and said third dummy lead-out contact hole are arranged in one line of said first direction.

18.(New) The semiconductor device according to claim 3, wherein said second gate is arranged parallel to said first gate.

19. (New) The semiconductor device according to claim 3, wherein said first dummy gate is arranged parallel to said first gate.

20. (New) The semiconductor device according to claim 3, wherein said second dummy gate is arranged parallel to said first gate.

21. (New) The semiconductor device according to claim 3, wherein said third dummy gate is arranged parallel to said first gate.

22. (New) The semiconductor device according to claim 5, wherein said second gate is arranged parallel to said first gate.

23. (New) The semiconductor device according to claim 5, wherein said first dummy gate is set parallel to said first gate.

24. (New) The semiconductor device according to claim 5, wherein said second dummy gate is set parallel to said first gate.

25.(New) The semiconductor device according to claim 5, wherein said third dummy gate is set parallel to said first gate.--

REMARKS

Applicant concurrently files herewith an Excess Claim Fee Payment Letter for excess dependent claims.

Claims 3-9 and 11-25 are all the claims presently pending in the application. Claims 1, 2, and 10 have been canceled above, and new claims 13-25 have been added to more completely define the invention. Claims 1-12 stand rejected on prior art grounds.

With respect to the prior art rejections, claims 1-3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hansch et al. (U.S. Pat. 6,174,741). Claims 4-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hansch et al., and further in view of Ham (U.S. Pat. 5,977,595).

These rejections are respectfully traversed in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the specification and